Remarks

This is a complete response to the Office Action mailed February 28, 2006. These remarks are proper, do not add new matter, and are not narrowing in response to a rejection over cited art, but rather serve to clarify Applicant's position that all claims are in condition for allowance.

In the event that the Examiner does not grant the reconsideration requested herein, the remarks further serve to explain why this case is not in condition for appeal.

Rejection Under Section 102

Claims 1-3, 7, 10-12, 16, 17, 20-22, 25, and 26 stand rejected as being anticipated by Staszewski '693. This rejection is respectfully traversed.

Claim 1

Applicant reiterates that the Examiner has not substantiated a prima facie case of anticipation in the record because Staszewski '693 does not identically disclose a *phase/frequency comparator...responsive to a transition location signal*. (see Applicant's Response of 11/28/2005, ppg. 13-18)

Applicant having obviated the previous anticipation rejection, the Examiner now finally rejects claim 1 by reading the *transition location signal* of the present embodiments onto the time-to-digital converter signal (TDC_RISE, TDC_FALL).

The Examiner's rejection is clearly reversible error because it relies on a flawed premise, that in order to construe a claim term in accordance with its ordinary meaning consistent with its usage in the specification requires an explicit definition of the claim term in the specification. (Office Action of 2/28/2006, pg. 6) Curiously, although

Examiner cites a lot of legal precedent in the Response to Arguments, none is cited here because none exists. Actually, the specification need not describe the invention *in haec verba*. That is, the specification "need not describe the claimed subject matter in exactly the same terms as used in the claims..." *Eiselstein v. Frank*, 52 F.3d 1035, 1038 (Fed. Cir. 1995).

Notwithstanding that, the Examiner's rejection is also clearly reversible error because it wrongly and blatantly states that the claim term *transition location signal* is not explicitly defined in the specification. (Office Action of 11/28/2005, pg. 6) The Examiner justifies doing so because the specification states "may be referred to" rather than "must be referred to." Again, where the Examiner otherwise provides legal citations abundantly, none is provided here because none exits. Actually, proper claim construction requires attaching the meaning when it is clearly defined in the specification. *In re Zletz*, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) In this case Applicant reiterates that the *transition location signal* is clearly defined as a single bit at the transition point of a falling edge (or rising edge) in the snapshot of the latch 302 (see Applicant's Response of 11/28/2005, pg. 14):

> N-bit parallel latch 302 latches in the outputs of N-bit tapped delay line 300 when reference clock signal 303 transitions (either from low to high or high to low, depending on the latch design). The output of N-bit parallel latch 302 is thus a snapshot of the progress of input signal 301 through N-bit tapped delay line 300 over one cycle of reference clock signal 303. This snapshot is fed into N-bit edge detect circuit 304, which is described in more detail in FIG. 4. N-bit edge detect circuit 304 outputs a single bit at the transition point of a falling edge (or rising edge, depending on the design) in the snapshot provided by N-bit parallel latch 302. This signal bit may be referred to as a transition location signal.
> (specification pg. 7 lines 1-10, emphasis added)

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Only a travesty of equities would require Applicant to appeal the issue of whether a claim term is clearly defined when it is explicitly defined in the specification.

The Examiner's rejection is also clearly reversible error because in seeking the "broadest reasonable interpretation consistent with the specification" the Examiner reaches an absurd conclusion. Applicant appreciates the Examiner's page-long recitation of the law explaining why he must find the broadest reasonable interpretation consistent with the specification. However, since this is a response to Applicant's previous arguments, it is curious that the Examiner does not reply to Applicant's point that his construction is unreasonable because it ignores both plain meaning and the explicit definition and usage in the specification of the claim term *transition location signal*. *In re Morris*, 43 USPQ2d 1753 (Fed. Cir. 1997). Particularly, Applicant argued in detail that the *transition location signal* plainly indicates a location snapshot of a transition, whereas Staszewski '693 discloses, and precisely the time-to-digital (TDC) signal indicates the relative timing snapshot between the reference transition signal 110 and the clock signal 114 (see Applicant's Response of 11/28/2005, ppg. 15-16):

> FIG. 6 is a timing diagram 600 associated with the time-to-digital converter 500 shown in FIG. 5. During a positive transition 602 of the reference oscillator FREF 110, the plurality of latch/registers 504 are accessed to obtain a snapshot 604 of the delayed replicas of the dVCO clock CDV 114 relative to the rising edge of the reference oscillator FREF 110. The snapshot 604 can be seen to express the time difference as a digital word.
> (Staszewski '693, col. 8 lines 39-46, emphasis added)

Ultimately, only a travesty of equities would require Applicant to appeal the issue of whether a *transition location signal* is reasonably anticipated by a time-to-digital converter signal, where the proposed claim construction ignores both the plain meaning of

the claim term and its definition and usage in the specification.

The Examiner's rejection is also clearly reversible error because it relies on the Examiner's mischaracterization of the cited reference. Particularly, the Examiner states:

> TDC_RISE, TDC_FALL is the transition location signal, since the snapshot taken by the parallel latches (504's in Fig. 5 of Staszewski) directly indicates the location of the feedback clock 114 through the tapped delay line 502's precisely at the occurrence of the feedback transition signal 110.
> (Office Action of 11/28/2005, pg. 7)

Nothing in Staszewski '693 discloses that the TDC converter 500 snapshot directly indicates the location of the transition as claimed in the present embodiments. As disclosed in the immediately preceding passage from Staszewski '693, for example, the snapshot 604 is a digital word indicating the time difference between the clock signal and the reference signal. Applicant reiterates that the TDC_RISE, TDC_FALL merely indicates which of the replicated reference cycles reflects the transition change at the snapshot. (see Applicant's Response of 11/28/2005, pg. 15) For example, in FIG. 6 of Staszewski '693 the TDC_FALL signal is associated with D(2). However, there are a number of different locations on either side of the reference signal transition 602 that would result in the same TDC_FALL signal of D(2). D(2) therefore does not indicate precisely the location of the transition as claimed in the present embodiments.

The Examiner's rejection is also clearly reversible error because it relies on the Examiner's mischaracterization of the present specification. Particularly, the Examiner states:

> Therefore, nothing in the specification indicates that the N-bit tapped delay line 300 initializes at the beginning of each clock reference 301 cycle.
> (Office Action of 11/28/2006, pg. 7)

The skilled artisan recognizes from a plain reading of the specification that in some embodiments the beginning of the propagations through the N-bit tapped delay line 300 is aligned precisely with a transition in input signal 301:

> FIG. 3 is a block diagram of a phase/frequency comparator design in accordance with a preferred embodiment of the present invention. Input clock signal 301 is fed to N-bit tapped delay line 300. N-bit tapped delay line 300 has N outputs, each of which duplicates input clock signal 301, but with incrementally increasing propagation delays. More specifically, if the outputs of N-bit tapped delay line 300 are numbered Q.sub.1, Q.sub.2, . . . Q.sub.N and the propagation delay of input signal 301 to output Q.sub.1 is equal to P, then the propagation delay to output Q.sub.2 is equal to P+U, where U is some unit delay time. Similarly, the propagation delay to output Q3 would be P+2U, the propagation delay to output Q.sub.4 would be P+3U, and so on. Thus, as a transition in input signal 301 propagates through delay line 300, the N taps or outputs of N-bit tapped delay line 300 reflect the propagation of this transition. For example, if N=5, and a transition from low to high (0 to 1) is made, delay line 300 will first output 00000, then 10000, then 11000, then 11100, then 11110, then finally 11111, at which the outputs of delay line 300 will remain until another transition in input signal 301 is made. One of ordinary skill in the art will recognize that N-bit tapped delay line may be implemented by connecting a number of non-inverting logic gates (e.g., buffers) in series and placing a tap between each two consecutive gates. (specification, para. [0023], emphasis added)

Only a travesty in equities would require Applicant to appeal this issue so readily understandable to the skilled artisan who simply reads the specification.

For at least these reasons the Examiner has failed to substantiate a prima facie case of anticipation because the cited reference fails to identically disclose all the features of the present embodiments as recited by the language of claim 1. Reconsideration and withdrawal of the present rejection of claim 1 and the claims depending therefrom are respectfully requested.

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Absent the requested reconsideration, a Pre-Appeal Brief Panel must find in the underlying facts "substantial evidence" that adequately supports the Examiner's legal conclusion of anticipation. This approach is consonant with the Office's obligation to develop an evidentiary basis for its factual findings to allow for judicial review under the substantial evidence standard that is both deferential and meaningful. *see In re Lee*, 277 F.3d 1338, 1344 (Fed. Cir. 2002).

Accordingly, this case is not in condition for appeal due to the unresolved factual issues that the Examiner has failed to make the requisite evidentiary showing in the record substantiating a prima facie case of anticipation, and due to the factual mischaracterizations of the cited reference and the specification, and due to the legal mischaracterizations asserted in the flawed attempt at a prima facie case of anticipation.

Claim 10

Applicant reiterates that the Examiner has not substantiated a prima facie case of anticipation in the record because Staszewski '693 does not identically disclose *encoding circuitry coupled to the phase detecting stage*. (see Applicant's Response of 11/28/2005, ppg. 18-20)

The Examiner's rejection is clearly reversible error because it relies on a flawed premise, that in order to construe a claim term in accordance with its ordinary meaning consistent with its usage in the specification requires an explicit definition of the claim term in the specification. (Office Action of 2/28/2006, pg. 8) Curiously, although Examiner cites a lot of legal precedent in the Response to Arguments, none is cited here because none exists. Actually, the specification need not describe the invention *in haec*

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verba. That is, the specification "need not describe the claimed subject matter in exactly the same terms as used in the claims..." *Eiselstein v. Frank.*

Notwithstanding that, the Examiner's rejection is also clearly reversible error because it wrongly and blatantly states that the claim term *encoding circuitry* is not explicitly defined in the specification. (Office Action of 11/28/2005, pg. 8) Actually, proper claim construction requires attaching the meaning when it is clearly defined in the specification. *In re Zletz.* In this case Applicant reiterates that the *encoding circuitry* is clearly defined in illustrative embodiments by the encoder 306 (see Applicant's Response of 11/28/2005, pg. 19):

> Weighted encoder 306 converts the output of N-bit edge-detect circuit 304 into a numerical phase difference value that reflects the phase difference between input signal 301 and reference signal 303.
> (specification pg. 7 lines 11-13)

Only a travesty of equities would require Applicant to appeal the issue of whether a claim term is clearly defined when it is explicitly defined in the specification.

The Examiner's rejection is also clearly reversible error because in seeking the "broadest reasonable interpretation consistent with the specification" the Examiner reaches an absurd conclusion. Particularly, Applicant argued in detail that the *encoding circuitry* plainly means an analytic process that changes the value of an input qualitatively, not quantitatively; whereas the NORM circuit of Staszewski '693 discloses a circuit that quantitatively changes an input (see Applicant's Response of 11/28/2005, ppg. 18-20):

> εt_r has to be normalized by dividing it by the clock period, in order to properly combine it with the integer phase detector output, θ_d.
> (Staszewski 693, col. 7 lines 21-24, emphasis added)

The Examiner's construction is unreasonable because it ignores both plain meaning

and the explicit definition and usage in the specification of the claim term *encoding circuitry*. *In re Morris*. Ultimately, only a travesty of equities would require Applicant to appeal the issue of whether *encoding circuitry* is reasonably anticipated by a normalization circuit, where the proposed claim construction ignores both the plain meaning of the claim term and its definition and usage in the specification.

The Examiner's rejection is also clearly reversible error because it relies on the Examiner's mischaracterization of the cited reference. Particularly, the Examiner states:

> The circuit (NORM) of Fig. 2 of Staszewski is an encoding circuitry since it converts the input digital signal into its equivalent binary code (column 5, line 64 through column 6, line 43).
> (Office Action of 11/28/2005, pg. 8)

Applicant agrees with Examiner to the extent that a circuit that converts an input digital signal into its equivalent binary value would affect the input qualitatively and not quantitatively, and thus would likely be characterizable as an encoding circuitry. However, nothing whatsoever in Staszewski '693 discloses that the NORM circuit does that function. The skilled artisan readily understands that any mathematical normalization process changes the input value quantitatively. In Staszewski '693, as seen in the passage above, the normalization process involves both division and addition steps. (see Applicant's Response of 11/28/2005, pg. 19) Nowhere in the passage relied on by the Examiner or anywhere else does Staszewski '693 disclose that the NORM converts the input digital value to an equivalent binary value, as the Examiner wrongly argues.

For at least these reasons the Examiner has failed to substantiate a prima facie case of anticipation because the cited reference fails to identically disclose all the features of the present embodiments as recited by the language of claim 10. Reconsideration and

withdrawal of the present rejection of claim 10 and the claims depending therefrom are respectfully requested.

Absent the requested reconsideration, a Pre-Appeal Brief Panel must find in the underlying facts "substantial evidence" that adequately supports the Examiner's legal conclusion of anticipation. This approach is consonant with the Office's obligation to develop an evidentiary basis for its factual findings to allow for judicial review under the substantial evidence standard that is both deferential and meaningful. *see In re Lee.*

Accordingly, this case is not in condition for appeal due to the unresolved factual issues that the Examiner has failed to make the requisite evidentiary showing in the record substantiating a prima facie case of anticipation, and due to the factual mischaracterizations of the cited reference, and due to the legal mischaracterizations asserted in the flawed attempt at a prima facie case of anticipation.

Claim 20

Applicant reiterates that the Examiner has not substantiated a prima facie case of anticipation in the record because Staszewski '693 does not identically disclose *a signal that corresponds to a transition location of the first signal....* (see Applicant's Response of 11/28/2005, ppg. 20-22) for the same reasons as discussed above for claim 1, which are incorporated herein but not repeated for brevity sake. Reconsideration and withdrawal of the present rejection of claim 20 and the claims depending therefrom are respectfully requested.

Absent the requested reconsideration, a Pre-Appeal Brief Panel must find in the underlying facts "substantial evidence" that adequately supports the Examiner's legal

conclusion of anticipation. This approach is consonant with the Office's obligation to develop an evidentiary basis for its factual findings to allow for judicial review under the substantial evidence standard that is both deferential and meaningful. *see In re Lee.*

Accordingly, this case is not in condition for appeal due to the unresolved factual issues that the Examiner has failed to make the requisite evidentiary showing in the record substantiating a prima facie case of anticipation, and due to the factual mischaracterizations of the cited reference and the specification, and due to the legal mischaracterizations asserted in the flawed attempt at a prima facie case of anticipation.

Rejection Under Section 103

Claims 8 and 18 stand rejected as being unpatentable over Staszewski '693 in view of Brachmann '154. This rejection is traversed because these claims are allowable as depending from an allowable independent claim, for reasons above, and providing additional limitations thereto. Reconsideration and withdrawal of this rejection are respectfully requested.

Allowable Subject Matter

Applicant acknowledges with appreciation the indication of allowability of claims 4-6, 13-15, 23, and 24. However, these claims are allowable as depending from an allowable independent claim, for reasons above, and providing additional limitations thereto. Accordingly, Applicant has opted not to place these allowable claims in independent form.

Conclusion

This is a complete response to the Office Action mailed February 28, 2006.

Applicant has also filed herewith a Request for Telephone Interview to be held before the Examiner makes the next action on the merits. In the event the Examiner does not grant the reconsideration requested herein, the interview is necessary to resolve the issues preventing this case from being in condition for appeal.

Should any questions arise concerning this response, the Examiner is encouraged to contact the below listed Attorneys.

Respectfully submitted,

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